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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,195	02/20/2004	Mou-Shiung Lin	MS98-002CCC CIPB	6169

7590 04/26/2006

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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 04/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/783,195	LIN ET AL.	
	Examiner	Art Unit	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *94-100,102,105-110,112-116,119,120,123,126-129 and 131* is/are pending in the application.

4a) Of the above claim(s) *94-100,102 and 105* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *106-110,112-116,119,120,123,126-129 and 131* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/09/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of claims 94-100, 102 and 205 in the reply filed on 29 Mar. 2006 is acknowledged. The traversal is on the ground(s) that the species given in the Office Acton would force the Applicant to bear the cost if the two separated species are separately examined and the filed of search must necessarily cover both species to provide a complete and adequate search. This is not found persuasive because the Applicant did not distinctly and specifically point out the supposed errors in the restriction requirement. Moreover, claimed invention is distinct from one to another as stated in the restriction mailed on 02/27/06. The Applicant is entitled to a single invention per application, 35 U.S.C. 121..

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 120, 126-129 and 131 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5665639 to Seppala.

Regarding claim 120, Seppala discloses a semiconductor chip or wafer in fig. 3d comprising: a silicon substrate200, col. 3 line 40, a first metallization structure 211, col. 3 line 38, over said silicon substrate 200, wherein said first metallization structure 211 comprises a first contact pad 211 (top portion surface); a passivation layer 220, col. 3 line 44, over said first metallization structure 211, wherein an opening in said passivation 220 layer exposes a top surface of said first contact pad 211; and a second contact pad 240 (bottom portion of 240) connected to said top surface, fig. 3d, wherein said second contact pad comprises a gold layer 240 with a thickness of between 2 and 100 micron, col. 7 line 12, and wherein said second contact pad is used to be wirebonded thereto, col. 10 line 1.

Regarding claims 126-128, Seppala discloses the semiconductor chip or wafer of claim 120, wherein said passivation layer 220 comprises a topmost nitride layer of said semiconductor chip or wafer, or wherein said passivation layer comprises a topmost oxide layer of said semiconductor chip or wafer, or wherein said passivation layer comprises a topmost CVD-formed layer of said semiconductor chip or wafer, col. 4 lines 56-61.

Regarding claims 129 and 131, Seppala discloses the semiconductor chip or wafer wherein said gold layer 240 is electroplated, col. 7 line 32, and further comprising a wirebond on said second contact pad 240, col. 9 line 61.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 106-110, 112-116 and 119 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6555459 to Tokushige et al in view of US 5665639 to Seppala et al.

Regarding claim 106, Tokushige discloses a semiconductor chip or wafer in fig. 6 comprising: a silicon substrate S, col. 5 line 2, a first metallization structure 1, col. 5 line 10, over said silicon substrate S; wherein said first metallization structure comprises a first contact pad (wherein 6 is located), a passivation layer 2/3, column 5 line 17, over said first metallization structure 1; wherein an opening in said passivation layer 2/3 exposes said first contact pad, fig. 6, and a second metallization structure 16, column 7

line 1, over said passivation layer 2/3, wherein said second metallization structure 16 comprises a copper layer having a thickness of between 2 and 100 μm (5 μm), col. 7 line 2, wherein said second metallization structure 16 comprises a second pad (where 18 is located) connected to said first pad, wherein the positions of said first and second contact pads from a top view are different.

But, Tokushige does not expressly disclose the second metallization layer 16 comprises gold.

However, Seppala discloses a method for fabricating a circuitry component comprising a thick gold layer 32, fig. 2, with a thickness of between 2 and 100 micron, col. 7 line 12. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use thickness of gold layer teaching of Seppala with Koike's method, because it would have created a more reliable and durable interconnect between the bump and the bonding pad as aught by Seppala, see abstract. Also, it would have been obvious to one of ordinary skill in art to use the thick gold layer teaching Koike and Seppala in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

Regarding claim 107-109, Tokushige discloses the semiconductor chip wherein passivation 2/3 comprises a topmost nitride layer, col. 7 line 25,of said semiconductor chip or wafer.

But, Tokushige does not disclose the passivation layer comprises a topmost oxide layer or a topmost CVD-formed layer.

However, Seppala discloses a semiconductor chip wherein passivation 220 comprises a topmost nitride layer or oxide layer or CVD-formed layer of the semiconductor chip or wafer, col. 4 line 59-61. At the time of the invention was made; it would have been obvious to one of ordinary skill in the art to use the nitride or oxide layer teaching of Seppala with Tokushige, because such passivation layer substitution would have been considered a mere substitution of art-recognized equivalent values, MPEP 2144.06

Regarding claim 110, Tokushige discloses the semiconductor chip or wafer wherein said second metallization structure16 further comprises a metal layer 6 under said gold layer copper layer 16

But, Tokushige does not disclose the metal layer 6 comprises Ti/W.

However, Seppala discloses a semiconductor chip in fig. 3d wherein gold layer 240, col. 3 line 63, comprises a TiW layer 231a, col. 5 line 57under said gold layer 240. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use TiW layer teaching of Seppala with Koike's method, because it would have created a more reliable and durable interconnect between the bump and the bonding pad as aught by Seppala, see abstract . In addition, the TiW would have improved the adhesion and provided barrier function.

Regarding claim 112-115, Tokushige discloses the semiconductor chip or wafer wherein said second contact pad is used to be wirebonded thereto, col. 5 line 13, and further comprising a wirebond and metal bump 7, col. 7 line 20, on said second pad, fig. 6.

Regarding claim 116, 119, Tokushige discloses the semiconductor chip or wafer further comprising a topmost polymer layer 3, col. 5 line 20, over said passivation layer 2/3, wherein said copper layer 16 over said topmost polymer layer 3, fig. 6, wherein said copper layer 16 is electroplated, col. 6 line 58-60.

With respect to gold layer, see discussion in claim 106.

7. Claim 123 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 5665639 to Seppala et al. et al in view of US 6555459 to Tokushige

Regarding claim 123, Seppala does not disclose the semiconductor chip or wafer further comprising a polymer layer over said passivation layer, wherein said second contact pad is over said polymer layer.

However, Tokushige discloses semiconductor chip or wafer in fig. 6 comprising a polymer layer 3, col. 5 line 20, over said passivation layer 2, col. 5 line 17, wherein a contact pad 16, col. 6 line 66, is over said polymer layer 3. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use polymer layer 3 teaching of Tokushige with Seppala's device, because it would have provided for making the height of solder uniform and such polymer layer would have a flat surface; thus the solder post can be formed accuratel as taught by Tokushige in col. 5 lines 20-30.

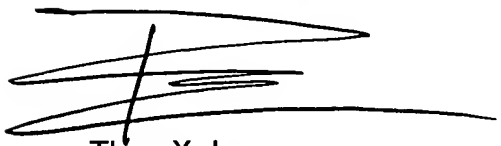
Regarding

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thao X. Le
21 April 2006